REMARKS/ARGUMENTS

In an Office Action dated March 22, 2007 claims 1–32 were rejected under § 103 based on Edsall in view of Testardi. Applicants amend the claims as shown above and submit that the claims are allowable.

Section 103 Rejections

Claim 17

Claim 17 is being treated as an exemplary claim in these remarks to better track the Office Action. The Office Action rejected claim 17 over Edsall and Testardi. Applicants respectfully traverse the rejection.

The rejection apparently somehow combines the basic data transfer capabilities of Edsall (connectors 302 and 204, MACs 304 and 322 and switches 306 and 320) and the fast path of Testardi, though how the two are combined is not stated. In fact, the Office Action defines the I/O modules to be the fast path of Testardi without any reference to Edsall. The Edsall pieces do not include the required processors in the I/O module, with the Testardi fast path apparently filling this requirement.

It might be argued that the various logic elements (302, 304, 306, 320, 322, 324) are all the required processors. Applicants first note that elements 302 and 304 are connectors. Edsall ¶ 0060. Clearly connectors cannot be processors. Elements 306 and 320 are switches. Edsall ¶ 0053. Clearly switches as used in Edsall are not processors. Elements 304 and 322 are Media Access Control (MAC) blocks. Edsall ¶¶ 0053, 0059. Clearly MAC blocks are not processors.

It might also be argued that Edsall teaches that a "multi-port switch will have virtualization logic separately implemented on one or more of its ports . . . rather than having centralized processing for all ports of a switch." While this may be a correct statement, none of the elements 302, 304, 306, 320, 322 or 324 do any such processing. Therefore Applicants submit that Edsall does not teach the required processors, with only the Testardi fast path apparently filling this requirement.

Applicants note that the claim specifically requires that the storage processing device may have the storage units directly connected or coupled through an external switch and the data

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migration is performed in either case. Applicants submit that the combination of Edsall and Testardi do not teach or suggest this requirement. The switches 306 and 320 of Edsall have been corresponded to being part of the I/O module, not the external switch required by the claims. Testardi is apparently cited for the processing in the I/O module as well as the control module with the required interactivity. However Testardi does not teach or suggest that the storage devices can be connected through a switch and have the processing of Testardi still be operational. Testardi indicates that the storage units must be directly connected to the storage processing device. Figure 4A of Testardi shows direct connection but at a general level. Figure 4B of Testardi is more specific and shows the hosts and storage units directly connected. Figure 4C adds external switches to Figure 4B but only hosts are attached to the switches, not storage units. There is no teaching or suggestion in Testardi that the storage units can be connected to the storage processing device through a switch and have the data migration operations still be successfully performed. While Edsall may show storage units connected to switches, this does not overcome the limitations of Testardi in this regard as the elements being used in Edsall do not contain any of the processing capabilities required in the claim and those processing capabilities are limited to directly connected storage units. Asserting that the storage units could be connected through a switch goes against the express teachings of Testardi and so would be an improper rejection.

It may be argued that the "may" creates alternative language so that if either condition is met, the rejection is proper. This misconstrues the language of the claim. Applicants reproduce the relevant language here for easier reference.

> a storage processing device coupled to the at least one switch and for coupling to the at least one host and the at least two storage units, where the host and the at least two storage units may be directly connected to the storage processing device or may be coupled to the storage processing device through the switch
>
> …
>
> a control module coupled to said input/output module, said input/output module and said control module being configured to interactively perform virtualization of a storage unit and migration of data between first and second storage units whether the at least one host and the at least two storage units are directly connected to the storage processing device or are coupled through the switch

From a reading of this language it is very clear that the "may" is not an alternative as to the operation of storage processing device. It is specifically required to operate in <u>both</u> conditions, not one. Thus this potential argument is misplaced.

It might also be argued that Testardi addresses the both conditions situation. Testardi ¶ 56 states "some or all of the connections by which the hosts, data management system 16 and data storage system 12 may be connected to the connection medium 18 may pass through other communication devices, such as a Fibre Channel switch . . ." While this is an accurate statement, it is inapposite to the situation at hand because the claims relate only to elements entirely <u>inside</u> the data storage system 12 of Testardi. The connections between the hosts and the data storage system are not at issue, except to note the citation only reinforces Applicants position on Figure 4C teaching that hosts can be attached to switches but not storage units.

Applicants thus submit that the combination of Edsall and Testardi do not teach or suggest all of the required claim elements. Therefore claim 17, and similar claims 1, 9 and 25, is allowable. Applicants submit that all of the present claims are allowable.

Claim 18

The Office Action alleges that Edsall shows the virtual target task and virtual initiator task of the processors of claim 18 as the commands to host and storage devices. Applicants traverse this rejection. First, as noted above, Edsall teaches none of the required processors so there can be no such tasks. Alternatively, none of the elements defined in claim 18 to be in the input/output module are processors which can perform tasks, so the limitations and requirements of claim 18 simply cannot be met by Edsall.

Applicants note that the claim requires specific, separate tasks of virtual initiator and virtual target. Edsall does not teach or suggest such a specific separation of tasks. Edsall only generally describes operations that are performed, not the details on how those mechanisms are performed.

As a result, Edsall does not and cannot teach or suggest processors in an input/output module performing the specified tasks so that the claim is allowable. As such, Edsall is not a proper reference for the specific required elements of claim 18, so that claim 18, and similar claims 2, 10, and 26, are allowable.

Claim 18 versus Claim 19

The Office Action did not address Applicants' argument that the rejections of claims 18 and 19 are inconsistent and request for clarification.

Applicants are aware that claims 18 and 19 do not depend from each other and that the claims are different so that a different rejection is proper. However, that does not allow identical terms to be construed differently in the two claims. The rejection of claim 19 states that the logic of virtual processor 308 is the virtualization processor of claim 19 and includes the virtual target, volume manager mapping block and virtual initiator. This is the only element in Edsall cited in claim 19 to support the rejection. Referencing then the rejection of claim 17, the virtual processor 308 is recited as corresponding to the control module. Taking this definition from claim 17 in combination with the fact that only the virtual processor 308 is cited in claim 19 as meeting the virtualization processor, it leaves no elements in the input/output module as forming part of the virtualization processor. That may meet claim 19, though Applicants do not concede the point, but comparing this effective definition that none of the virtualization processor is in the input/output module to the allegation in the rejection of claim 18 that the input/output module includes a processor that performs virtual initiator and virtual target tasks, which are clearly virtualization processes, shows the inconsistency. The rejection of claim 19 characterizes the virtualization as being done only in the control module but claim 18 requires virtualization tasks in the input/output module. Thus the rejections of the two claims are inconsistent. Therefore one of the two rejections is improper and must be withdrawn. Applicants leave it to the Examiner to select one but submit that one must be withdrawn.

Claim 19

In rejecting claim 19, as noted above, there is no recitation of any elements of Edsall to correspond to the input/output module of the claim. Thus a required element is not defined. Further claim 19 requires specific elements, not just general allegations. Applicants submit that merely having addresses (and clearly that a switch does not have an address) is insufficient to meet the specific claim requirements so that claims 19, 3, 11 and 27 are allowable.

Claim 21

The arguments from claim 18 apply equally to claim 21 and its similar claims.

Related Application

Applicants specifically wish to draw attention to co-pending U.S. Patent Application No. 10/695,408, currently on appeal and which has been terminally disclaimed against the instant application.

CONCLUSION

Entry of the amendments is requested as they place the application in condition for allowance. Based on the above Applicants respectfully submit that all of the present claims are allowable.

<div align="center">Respectfully submitted,</div>

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